5.8. Common-collector amplifier.

Circuit description. The common-collector amplifier is used for coupling circuits with small driving capabilities with heavy loads. The voltage gain of the amplifier is less than but close to unity; the current gain is however nearly 1+β. Due to this property, the amplifier can be considered as a power amplifier and is often used for driving low load impedances such as speakers, motors, etc. The circuit's schematic is shown in Figure 5.17.
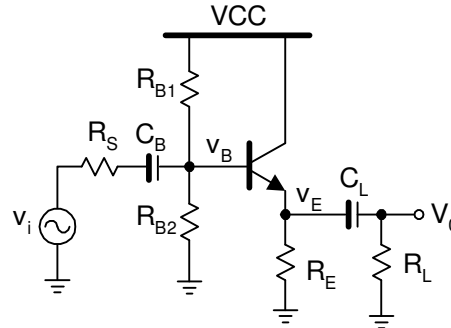

Fig. 5.17. Common-collector configuration: signal is injected at the base terminal and output is at the emitter terminal.

For DC analysis, the AC input signal is short circuited, and the capacitors are replaced by open circuits. The equivalent circuit is shown in Fig. 5.18a. Resistors RB1 and RB2 together with the effect of VCC can be replaced by an equivalent circuit as depicted in figure 5.18b. The equivalent voltage VB and RB are

$$V_{BB} = \left(\frac{R_{B2}}{R_{B1} + R_{B2}} \right) VCC = \left(\frac{R_B}{R_{B1}} \right) VCC \tag{5.30}$$

$$R_B = \frac{R_{B1} R_{B2}}{R_{B1} + R_{B2}} \tag{5.31}$$

The base and emitter currents are related by the following expression

$$V_{BB} = R_B I_{BQ} + 0.7 + R_E I_{EQ} = 0.7 + \left(\frac{R_B}{\beta} + \left(\frac{1+\beta}{\beta} \right) R_E \right) I_{CQ} \tag{5.32}$$

and the equation for the transistor's output yields,

$$VCC = V_{CEQ} + R_E I_{EQ} = V_{CEQ} + \alpha R_E I_{CQ} \tag{5.33}$$
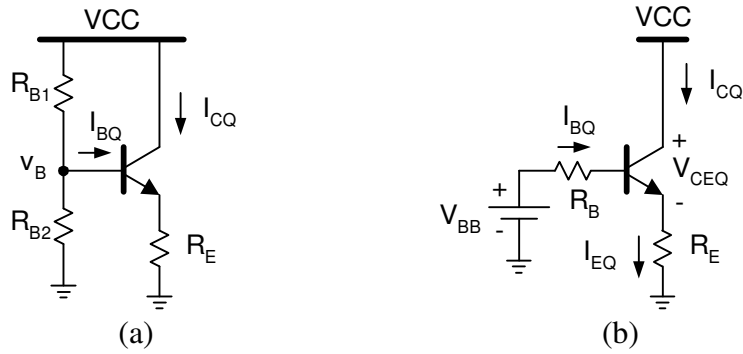
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Fig. 5.18. a) Common-collector equivalent circuit for DC analysis, and b) modified equivalent circuit.

The AC equivalent circuit is obtained for Fig. 5.17 by making VCC=0 and replacing the transistor by its small signal model. It is easier to find the solution of the circuit if the T-model is used, as depicted in Figure 5.19a. Similarly to the common-emitter configuration, the small signal transfer function presents two poles due to the coupling capacitors C_B and C_L, and the resistors associated with them. At the medium frequency band where the capacitors can be considered as short circuits, the simplified equivalent circuit shown in Fig. 5.19b results.
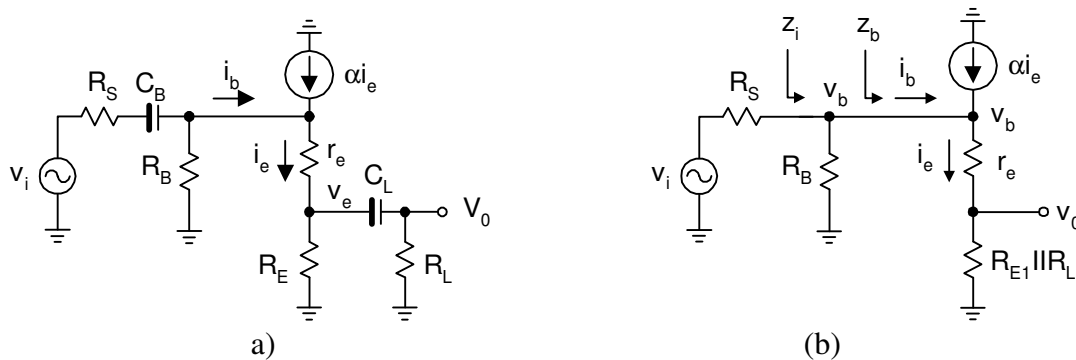

Fig. 5.19. Small signal model for the common-collector amplifier: a) including the AC coupling capacitors, model valid for low and medium frequencies, and b) small signal model valid for medium frequencies only; the poles introduce by the capacitors are ignored.

The amplifier's input impedance z_b is defined as follows

$$z_b = \frac{v_b}{i_b} = \frac{v_b}{\dfrac{i_e}{1+\beta}} = (1+\beta)\left(\frac{v_b}{\dfrac{v_b}{r_e + R_E \parallel R_L}}\right) = (1+\beta)(r_e + R_E \parallel R_L) \qquad (5.34)$$

Notice that the **input** *impedance measured at the base of the transistor is determined by the overall resistance seen at the emitter terminal, in this case $r_e + R_{E1} \parallel R_L$ multiplied by the emitter-base current gain $1+\beta$.* It is interesting to notice that equation 5.34 can be expressed as

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$$z_b = r_\pi + (1+\beta)(R_E \| R_L) \tag{5.34b}$$

This is an important property of circuits with emitter resistance: the resistors attached at the emitter terminal increase the input impedance seen at the base terminal by a factor $(1+\beta)(R_{E1}\|R_L)$. The overall input impedance seen by the input voltage source v_i is then

$$z_i = R_B \| z_b = R_B \| (r_\pi + (1+\beta)(R_E \| R_L)) \tag{5.35}$$

The voltage v_b is generated from the input voltage and the voltage divider due to R_S, R_B and z_b as

$$\frac{v_b}{v_i} = \frac{z_i}{R_S + z_i} \tag{5.36}$$

To avoid signal attenuation at the input stage, it is desirable to design the circuit such that $R_S \ll z_i = z_b \| R_B$. As aforementioned, the impedances connected at the emitter help us to this end. From fig. 5.19, it can be noticed that the output voltage is generated from v_b as follows:

$$\frac{v_o}{v_b} = \frac{R_E \| R_L}{r_e + R_E \| R_L} \tag{5.37}$$

By using equations 5.35 and 5.36, the overall voltage gain can be obtained as

$$\frac{v_o}{v_i} = \left(\frac{v_b}{v_i}\right)\left(\frac{v_o}{v_b}\right) = \left(\frac{z_b \| R_B}{R_S + z_b \| R_B}\right)\left(\frac{R_E \| R_L}{r_e + R_E \| R_L}\right) \tag{5.38}$$

The amplifier's voltage gain is less than unity, and it is composed by the multiplication of two attenuation factors: the input and output attenuators. The effect of the input voltage source impedance R_S is to reduce the overall transfer function, and its effect is minimized if the input impedance of the amplifier is much larger then R_S. As a rule of thumb, the attenuation factor is minimized if the conditions $z_b\|R_B \gg R_S$ and $R_{E1}\|R_L \gg r_e = V_{th}/I_{EQ}$ are satisfied. While to satisfy the former condition is relatively easy in most of the practical designs, this is not the case for the latter one since R_L could be very small; for instance 8 Ω for many speakers. For an emitter resistance r_e ($=0.025/ I_{EQ}$) equal to 8 Ω an emitter current of 3.125 mA. Under these conditions, equation 5.38 leads to an overall voltage gain of less than 0.5. What current is needed if a voltage gain of 0.9 is required? The emitter resistance re must be equal to 0.8 Ω leading to an emitter current of roughly 31 mA. What about driving a 4 Ω speaker?
The fundamental equations for the common-collector structure are: 5.30-5.32 for the DC analysis, and 5.35 and 5.38 for the AC behavior. It is left to the reader to demonstrate that the *current gain of this topology is close to β_{AC}* if the amplifier is properly designed; hence the *power gain might be close to β_{AC}* as well.

5.9. Common-base amplifier.

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Contrary to the previous topologies, in the common-base configuration, the input signal is injected into the emitter while the output is at the collector terminal, as shown in the following schematic. The base terminal is AC-grounded through a large capacitor CB connected between transistor's base and ground. The DC blocking capacitors CI and CL are used to make the biasing of this stage independent of the previous and following amplifiers; these capacitors introduce low-frequency pole-zero pairs, and their values should be increased as much as possible to push the poles to very low frequencies.

The DC analysis of the circuit is similar to the analysis of previous circuits; from the equivalent circuit for DC analysis only, we get the equivalent circuit depicted in Fig. 5.21a. The equivalent base voltage V_{BB} and base resistor R_B are given by

$$V_{BB} = \left(\frac{R_{B2}}{R_{B1}+R_{B2}}\right)VCC = \left(\frac{R_B}{R_{B1}}\right)VCC \qquad (5.39)$$

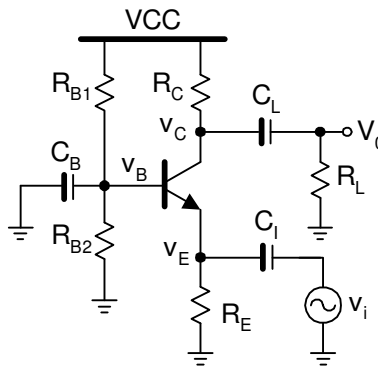$$R_B = \frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} \qquad (5.40)$$

Fig. 5.20 Common-base amplifier based on a BJT.

The base and emitter currents are related by the following expression

$$V_{BB} = R_B I_{BQ} + 0.7 + R_E I_{EQ} = 0.7 + \left(\frac{R_B}{\beta} + \left(\frac{1+\beta}{\beta}\right)R_E\right)I_{CQ} \qquad (5.41)$$

and the equation of the output stage yields,

$$VCC = V_{CEQ} + R_C I_{CQ} + R_E I_{EQ} = V_{CEQ} + (R_C + \alpha R_{E1})I_{CQ} \qquad (5.42)$$

The AC small signal analysis can be carried out by using the π-hybrid or the T-model. Since the input signal is applied to the emitter terminal, it is easier to visualize circuit's properties if the T-model is used. Assuming that the DC blocking capacitors are large, the poles generated by C_B, C_I and C_L are located at very low frequencies. At the medium band frequencies, where the effect of

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these poles can be ignored, the equivalent depicted in Fig. 5.21b results. Since the base terminal is grounded, it can be seen that the input impedance is then

(a)   (b)
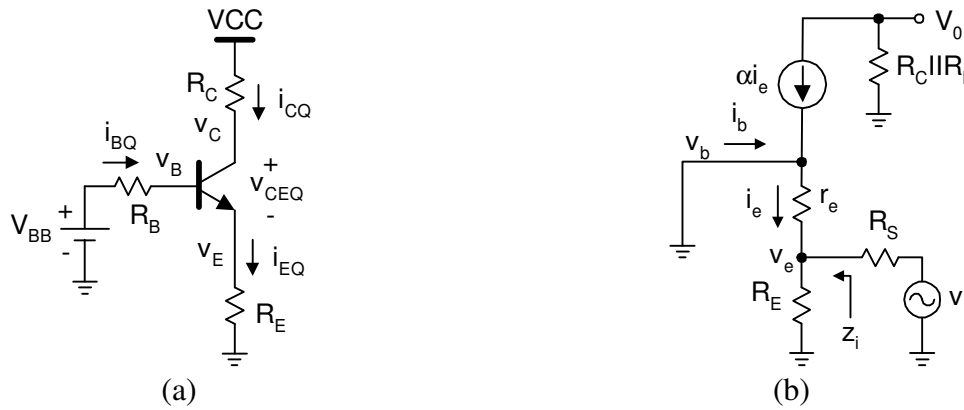
5.21. Common-base configuration: a) DC-equivalent circuit and b) small signal equivalent circuit for AC analysis for medium band frequencies.

$$z_i = \frac{v_e}{i_i} = r_e \parallel R_E = \frac{r_e R_E}{r_e + R_E} = \frac{r_e}{1 + \dfrac{r_e}{R_E}} \tag{5.43}$$

Since $r_e = V_{th}/I_{EQ} = \alpha V_{th}/I_{CQ} = \alpha/g_m$. If R_E is selected such that $R_E \gg r_e$ then the input impedance is dominated by the emitter resistance r_e, leading to the following important result:

$$z_i \cong r_e = \frac{\alpha}{g_m} = \frac{\alpha V_{th}}{I_{CQ}} \qquad\qquad \text{if } \frac{r_e}{R_E} = \frac{\alpha}{g_m R_E} = \frac{\alpha V_{th}}{I_{CQ} R_E} \ll 1 \tag{5.43b}$$

At room temperature, this result yields,

$$z_i \cong r_e = \frac{\alpha}{40 * I_{CQ}} \qquad\qquad \text{if } \frac{\alpha}{40 * I_{CQ} R_E} \ll 1 \tag{5.43c}$$

Therefore, the input impedance of the common-base configuration can be made very small by increasing the collector current. This is a very important property of the common-base configuration, and it is often exploited in transimpedance amplifiers where the input signal is current. Sensors such as photodiodes, and photo-transistors used in optical communication systems convert the photonic energy into AC current that must be converted into voltage; common-base amplifiers are well suited for such applications. Another quite important application, discussed at the end of this chapter, is the so-called cascode structure used to increase the output impedance of the amplifier.

Since the base terminal is AC grounded, the emitter current is fully determined by the transistor's emitter resistance and the input voltage; $i_e = -v_e/r_e$. Therefore, the collector current is also proportional to the emitter voltage, leading to the following transfer function

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$$\frac{v_o}{v_b} = \left(\frac{-i_c}{v_e}\right)(R_C \parallel R_L) = \left(\frac{-\alpha i_e}{v_e}\right)(R_C \parallel R_L) = \frac{R_C \parallel R_L}{r_e} \tag{5.44}$$

The emitter resistance is determined by the DC emitter current and the thermal voltage, hence equation 5.43 can be simplified as

$$\frac{v_o}{v_e} = (R_C \parallel R_L)\frac{I_{EQ}}{V_{th}} = (R_C \parallel R_L)\left(\frac{g_m}{\alpha}\right) \cong (R_C \parallel R_L)g_m \tag{5.44b}$$

Notice that this equation is similar to that of the common-emitter transistor; the main difference of the two structures is the input impedance: usually the input impedance of the common-emitter configuration is large, especially if an additional resistor is added to the emitter terminal. The common-base configuration presents very small input impedance that makes it a very attractive solution for current-mode sensors such as photo-detectors.

The overall voltage gain taking into account the resistance of the input voltage source is obtained from Fig. 5.21b and equation 5.44 as

$$\frac{v_o}{v_i} = \left(\frac{z_i}{R_S + z_i}\right)\left(\frac{R_C \parallel R_L}{r_e}\right) \tag{5.45}$$

The fundamental equations for the 3 topologies are summarized in the following table.

Parameter	Common-emitter Fig. 5.22 part Va	Common-Collector Fig. 5.17	Common-Base Fig. 5.20
DC Equations	$V_{BB} = 0.7 + I_{CQ}\left(\frac{R_B}{\beta} + \left(\frac{1}{\alpha}\right)(R_{E1} + R_{E2})\right)$ $VCC = V_{CEQ} + I_{CQ}\left(R_C + \frac{R_{E1}+R_{E2}}{\alpha}\right)$	$V_{BB} = 0.7 + \left(\frac{R_B}{\beta} + \left(\frac{1+\beta}{\beta}\right)R_{E1}\right)I_{CQ}$ $VCC = V_{CEQ} + \alpha R_{E1}I_{CQ}$	$V_{BB} = 0.7 + \left(\frac{R_B}{\beta} + \left(\frac{1+\beta}{\beta}\right)R_E\right)I_{CQ}$ $VCC = V_{CEQ} + \left(R_C + \frac{R_{E1}}{\alpha}\right)I_{CQ}$
Input impedance	$z_i = (r_\pi + (1+\beta)R_{E1}) \parallel R_B$	$z_i = (r_\pi + (1+\beta)(R_E \parallel R_L)) \parallel R_B$	$z_i = r_e \parallel R_E$
Voltage gain	$A_V = -\left(\frac{z_i}{R_S + z_i}\right)\left(\frac{\alpha(R_C \parallel R_L)}{r_e + R_{E1}}\right)$	$\frac{v_o}{v_i} = \left(\frac{z_i \parallel R_B}{R_S + z_i \parallel R_B}\right)\left(\frac{R_E \parallel R_L}{r_e + R_E \parallel R_L}\right)$	$\frac{v_o}{v_i} = \left(\frac{z_i}{R_S + z_i}\right)\left(\frac{R_C \parallel R_L}{r_e}\right)$

Table 5.1 Fundamental equations for the common-emitter, common-collector and common-base configurations.

5.10. Amplifier's design considerations using bipolar devices.

Design of a large gain amplifier using a common-emitter structure with limited input impedance: A graphical approach. A major concern of the analog circuit designer is what should be the acceptable range of values for a set of given specifications? This part of the design is obscure in most of the existing literature, and that is the reason why novel designers think that analog design is a kind of black art. In fact the selecting a proper operating point is not a trivial task, since there are many parameters and constraints involved. However, as shown in this

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section, a simple graphical approach can help us to understand all design issues involved and to end up with reasonable solutions.

A couple of design examples are discussed in this section. The first one deals with the use of the simplified common-emitter configuration shown in Fig. 5.50a for the design of an amplifier with voltage of -20 V/V driving a load impedance of 10 kΩ. First of all, the limitations due to signal swing must also be incorporated as design constraints. Usually those conditions impose some boundary conditions to the circuit's solution. Among the equations given in table 5.1, the following design constraints are added.

i)   Expected maximum output swing V_{omax}
ii)   Required voltage gain A_V
iii)   Input and load impedances to be driven
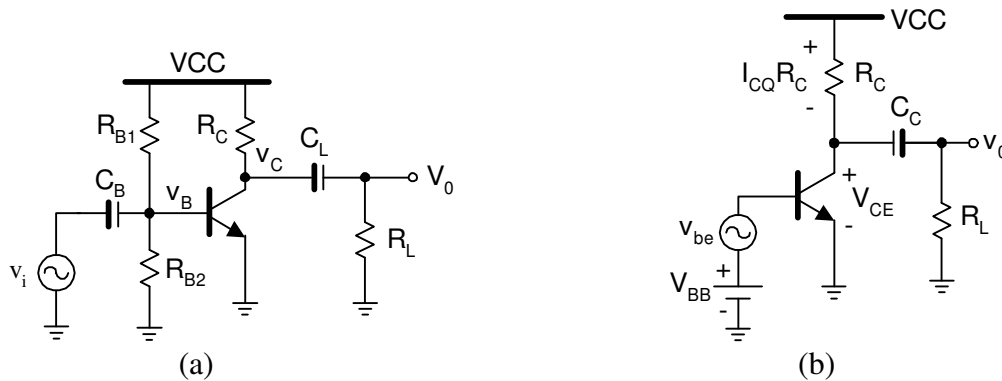iv)   Supply voltage

Fig. 5.50. Common-emitter amplifier.

Although the input impedance is not considered in this case, it will be incorporated to the design equations in the following subsection. The following equations define the operating point of the amplifier's output stage. For the DC signal, as discussed in previous subsections and depicted in table 5.1, at the collector-emitter terminals we have

$$V_{CC} = V_{CEQ} + I_{CQ}R_C \tag{5.46}$$

The collector-emitter voltage V_{CEQ} *must be large enough to tolerate the signal variations*. Hence, $V_{CEQ} > V_{CESAT} = 300$ mV to keep the transistor operating in linear region. To leave some room for potential temperature variations and components tolerances, let us consider a minimum V_{CEQmin} voltage of 500 mV. Therefore, the selected V_{CEQ} voltage must be such that under the most negative swing at the amplifier's output, the collector-emitter voltage is greater or equal than 500 mV. This condition is expressed as

$$I_{CQ} < \frac{V_{CC} - V_{o\,max} - 0.5}{R_C} \tag{5.47}$$

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On the other hand, V_{CEQ} can not be close to VCC otherwise we do not have room for the positive signal swing. The voltage drop across the collector resistor R_C ($I_{CQ}R_C$) must be greater than V_{omax}, leading to the following bound for the collector current

$$I_{CQ} > \frac{V_{omax}}{R_C} \tag{5.48}$$

Another important parameter is the small signal voltage gain from transistor's base to amplifier's output. From our previous analysis, the voltage gain is given by

$$\left|A_V\right| = \left|\frac{v_0}{v_{be}}\right| = g_m(R_C\|R_L) = \frac{I_{CQ}(R_C\|R_L)}{V_{th}} \tag{5.49a}$$

or

$$I_{CQ} = \left(|A_V|V_{th}\right)\left(\frac{R_C + R_L}{R_C R_L}\right) \tag{5.49b}$$

These equations can be plot in the I_C-R_C plane as shown in the following figure. Equations 5.47 and 5.48 represent the boundaries for the acceptable solutions, and 5.49b is the actual solution for the amplifier's voltage gain. These plots are function of the required voltage gain A_v and the load impedance R_L. In Figure 5.51, equation 5.49b is plotted for 4 different amplifier's gain (A_V = -10, -20, -40 and -100). Notice that the solution's boundaries (equations 5.47 and 5.48) are independent of the desired voltage gain; these equations however are determined by the maximum voltage swing expected at the amplifier's output. The results shown in the figure below are generated by using V_{CC}= 5V, V_{omax}=1 V_{peak} and V_{th}=26 mV and R_L=10KΩ.
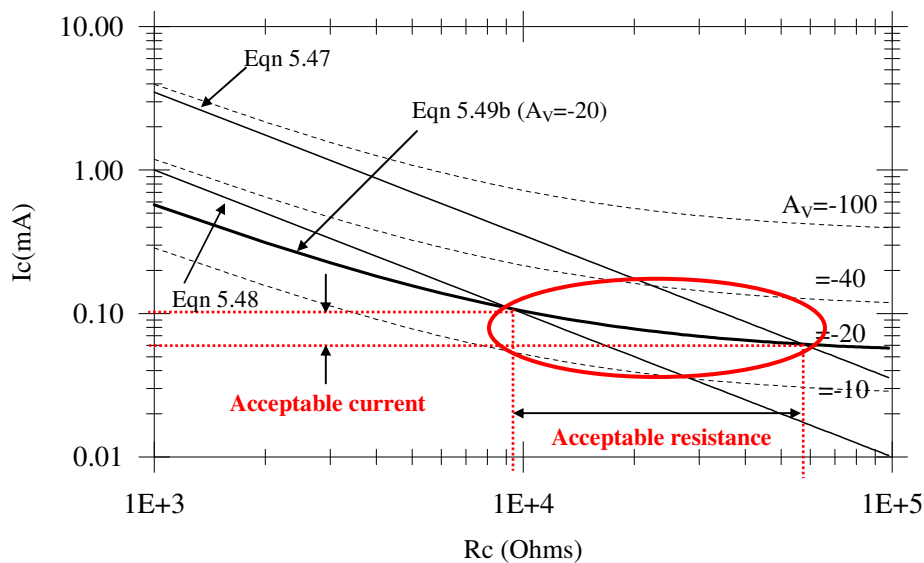

Fig. 5.51. I_C-R_C plane shown acceptable region.

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Notice in this plot that the acceptable region is quite limited for large voltage gains. According to these results it is clear that we can not design a voltage amplifier with gain of –100 for the given supply voltage and the desired output voltage swing. The solution for equation 5.49b does not intersect the acceptable region. For the case of an amplifier with voltage gain of -20, for instance, we can achieve the specifications (all design constraints are satisfied) if and only if the collector resistance is in the range of 9.5kΩ till 58 kΩ. The quiescent collector current must be in the range of 60μA-100μA. Another advantage of using this approach is that the power consumption can be easily optimized by selecting the largest possible collector resistor R_C. For practical applications, however, it is always good practice to overdesign the amplifier in order to accommodate both temperature variations and tolerances of the devices and components used.

Once the output stage of the circuit is defined and the collector current determined, the base current can be computed. For amplifiers built using discrete components, there is a complete family of devices that can be used. The resistors attached to the base terminal can be computed based on the amount of base current needed and the input impedance required. There are two basic equations (see table 5.1, common-emitter configuration with $R_{E1}=R_{E2}=0$) and two unknowns; hence we do not have any degree of freedom for optimization. These equations are repeated here for sake of completeness. From the DC analysis we have:

$$\left(\frac{R_B}{R_1}\right)VCC = I_B R_B + 0.7 \tag{5.50}$$

and the amplifier's input impedance (AC analysis) is given by:

$$Z_{in} = r_\pi \| R_B = \frac{r_\pi R_B}{r_\pi + R_B} = \frac{r_\pi}{1 + \dfrac{r_\pi}{R_B}} = \frac{r_\pi}{1 + \dfrac{r_\pi}{R_B}} \tag{5.51}$$

If $R_B \gg r_\pi$, the effect of the bias network becomes negligible on the input impedance, and it is dominated by the transistor's base-emitter resistance r_π. For practical applications it is common practice to increase as much as possible the input impedance. Thus, selecting a high-beta transistor helps. Large β reduces the base current and increases the input impedance of the amplifier ($r_\pi = V_{th}/I_{BQ}$) but in most of the cases high-β devices have limited current capabilities, and are used as preamplifiers. Typically the transistors used as power amplifiers have limited β; e.g. less than 50. Also, if we select the least possible collector current, the required base current reduces and that increases the input impedance and the power consumption reduces as well.

Numerical example. For a gain amplifier of –20 V/V and $V_{omax}=1$ V_{pk}, from figure 5.51, we select $I_C=80$ μA and $R_C=12$ kΩ. For this collector current, the beta of the 2N2222 is close to 150, therefore the DC base current is around 0.8 μA. The base-emitter resistance r_π is around 47 kΩ. Therefore R_B can be selected around 300 kΩ and the overall input impedance is around 40 kΩ. Let us use for this exmple $R_B=400$ kΩ; then $V_B=0.6+I_B R_B=0.82$ V. Since the base current is very small, for our hand calculations we use $V_{BE}=0.6$ V rather than 0.7 V; anyway, the base-emitter voltage must be obtained from SPICE results, and the resistors should be adjusted accordingly. After some basic algebra, the value of the resistors lumped to the base terminal are

determined as R_{B1}=2.2 MΩ, and R_{B2}=490kΩ, respectively. Spice waveform at the transistor's collector is shown below.
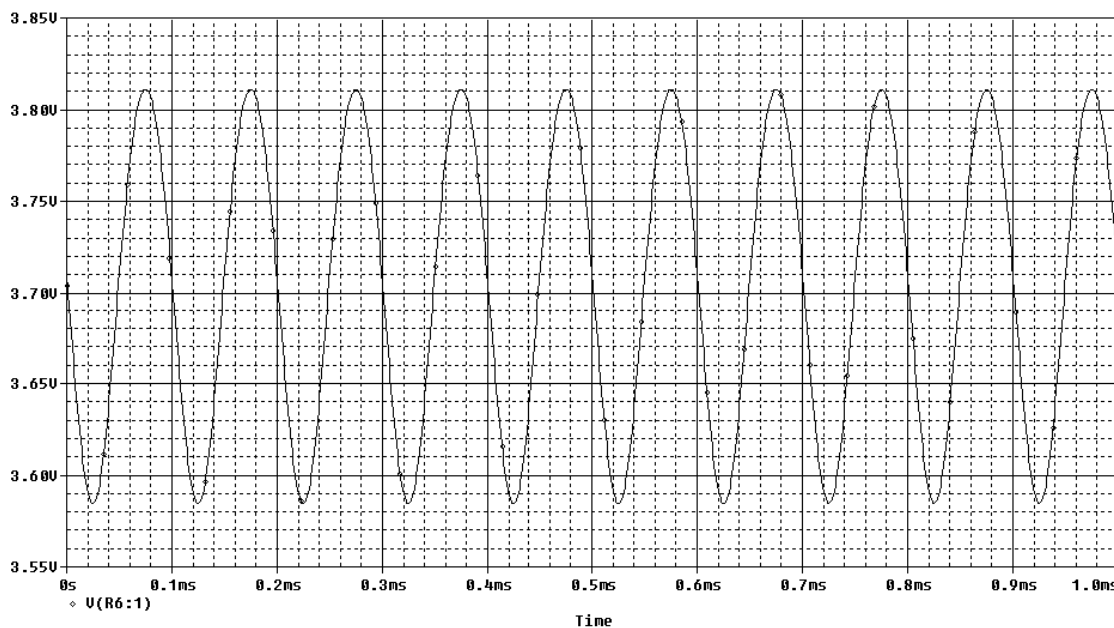

Fig. 5.52. Signal waveform at the collector terminal of the BJT. The input signal is 5 mV$_{pk}$ and the voltage gain is 23.5 V/V.

The voltage gain is 15 % larger than the expected one; analyzing the Spice output file we found that the β-ac is 15 % larger than the value used for our hand-calculations. As a result, the DC collector current is also 15% larger, which is evident in Fig. 5.52 analyzing the DC voltage component (average); it is around 3.7 V instead of the expected 4 V (=V_{CC}-12kΩ*80 μA). If needed, using the β obtained from the Spice output file, the base current and resistors lumped to the base can be re-calculated.

Although large volatge gain can be obtained with the previous topology, the input signal must be limited to 10 mV, otherwise the small signal approximations are no longer valid. There are two main limitations with this topology: a) the input signal appears directly across the base-emitter terminals, limiting the amplitude of the input signals for linear operation and b) the input impedance is determined by the base-emitter resistance which is not very high. A 20 mV input signal was applied to the previous circuit; the spice results are shown in figure 5.53 and 5.54. Notice that the ouput waveform is not even close to a sinusoidal output. A fourier analysis of this waveform, carried out using the transient simulation option available in Spice, reveals that the fundamental component has an amplitude of roughly 500 mV while the second harmonic component is 80 mV. The second harmonic distortion is rougly 16%, that is not small enough for most practical applications; equation 5.10 predicts HD2 ≈ 20%, which is relativelty close to Spice results. The third harmonic component is 10 mV, leading to a HD3=2%, same value is predicted by equation 5.10.
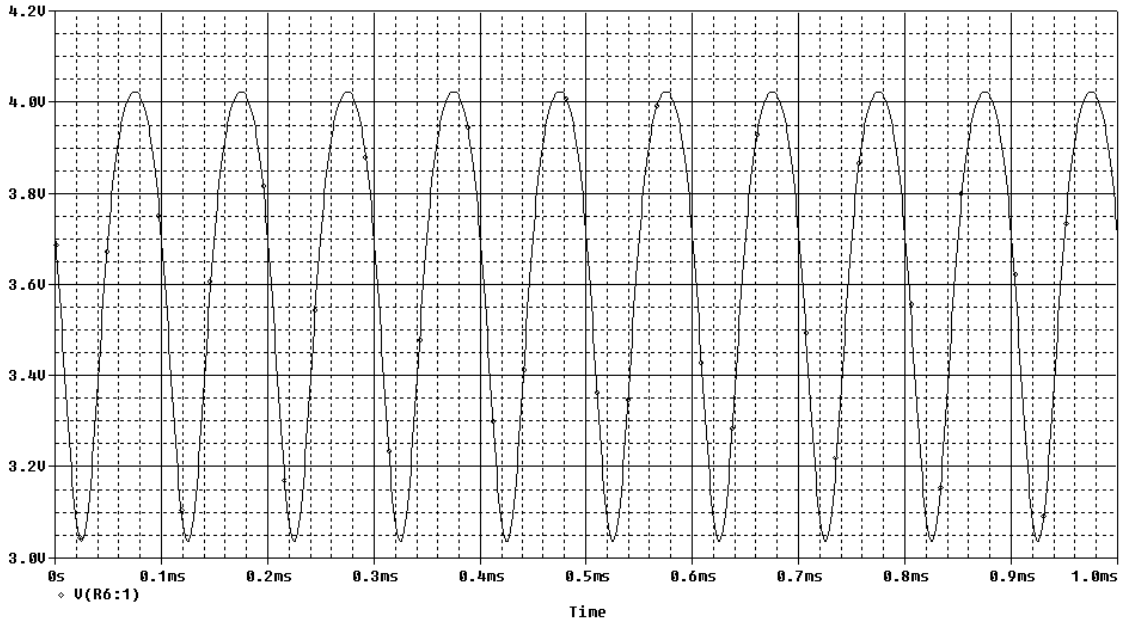
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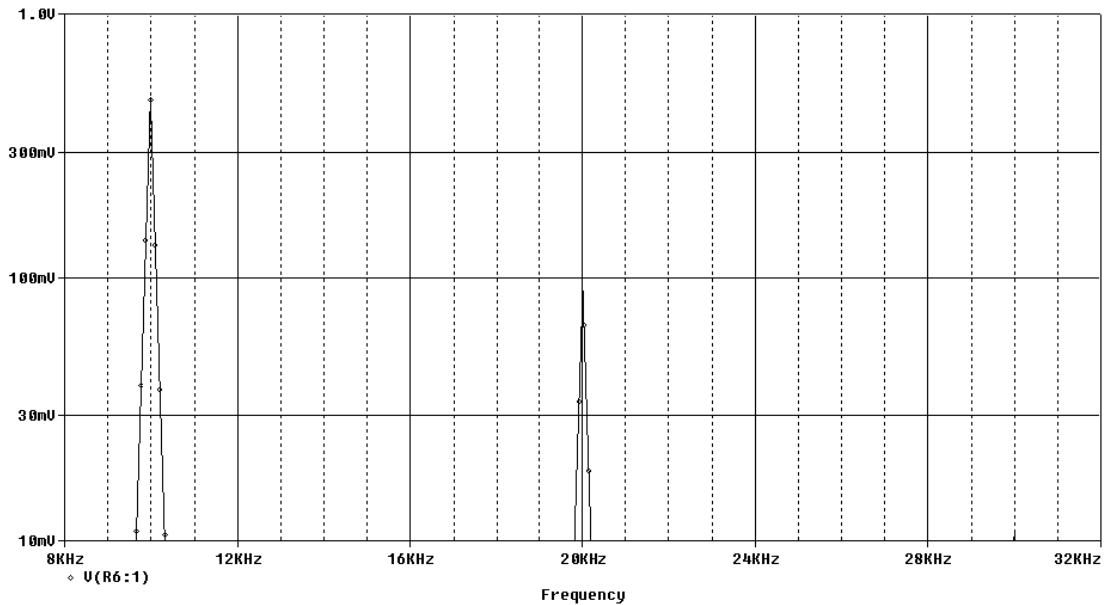Fig. 5.53. Output waveform for an input signal of 20 mV$_{pk}$.

Fig. 5.54. Harmonic components for the output waveform shown in Fig. 5.53; HD2 is the most critical distortion component in this example.

Example 2. Design of a common-emitter amplifier with larger input impedance but limited voltage gain. In practical applications, the amplifier's input impedance is also an important design parameter. The AC input impedance can be increased if an emitter resistance is added, as shown in Fig. 5.55. The DC and AC equations are given in table 5.1, with $R_{E1}=R_E$ and $R_{E2}=0$.

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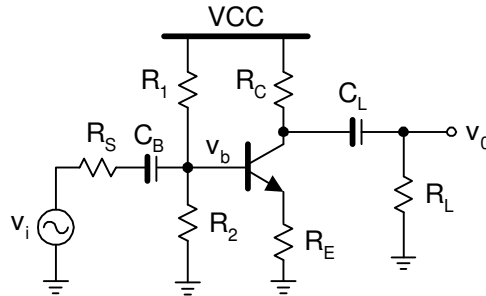
5.55. Common-emitter amplifier with emitter resistor.

In the following analysis we assume that $R_B \gg \beta R_E \gg r_\pi$. The input impedance of this topology is given as:

$$Z_i = (r_\pi + \beta R_E) \| R_B \cong \beta R_E \tag{5.52}$$

R_B slightly reduces the overall amplifier's voltage gain. For the 4-resistor amplifier, the set of equations that describe its DC and AC operation are obtained as follows:

$$I_{CQ} = \frac{V_{CC} - V_{CE}}{R_C + \dfrac{R_E}{\alpha}} \leq \frac{V_{CC} - V_{o\,max} - 0.5}{R_C + \dfrac{Z_i}{\beta}} \tag{5.53}$$

The condition $V_{CE} > v_{omax} + 0.5$ guarantees that the BJT stays in linear region under maximum signal variations. To avoid signal clipping for positive output swing, the collector voltage has to be properly selected; the circuit must be able to handle voltage variations of at least V_{omax}, then

$$I_{CQ} > \frac{V_{o\,max}}{R_C} \tag{5.54}$$

Form the small signal analysis of the circuit, the amplifier's voltage gain is determined by the following expression

$$|A_V| = \left| \frac{v_0}{v_b} \right| = \frac{g_m (R_C \| R_L)}{1 + g_m R_E} = \frac{\dfrac{I_{CQ}}{V_{th}} (R_C \| R_L)}{1 + \dfrac{I_{CQ}}{V_{th}} R_E} \tag{5.55a}$$

In this expression *we are not including the input voltage resistance R_S*, but it can be easily incorporated to expression 5.55a.
Notice that the resistor attached to the emitter reduces the overall voltage gain according to the ratio of the voltage drop across R_E and the thermal voltage. This equation can also be re-written in the following form:

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$$I_{CQ} = \frac{|A_V| V_{th}}{\dfrac{R_C R_L}{R_C + R_L} - |A_V| R_E} \cong \frac{|A_V| V_{th}}{\dfrac{R_C R_L}{R_C + R_L} - \dfrac{|A_V| Z_i}{\beta}} \tag{5.55b}$$

This equation clearly indicates that **the selection of I_{CQ} is not a trivial task**, because it is a function of the required voltage gain, AC load impedances $R_C \| R_L$ and required input impedance. Another critical design consideration is the amount of current provided by the BJT to support the output swing variations with small distortion. The maximum AC current provided by the BJT to the load impedance R_L and collector capacitor R_C is determined by the largest output swing required, therefore

$$i_{c\,max} = \frac{v_{o\,max}}{\dfrac{R_C R_L}{R_C + R_L}} \tag{5.56}$$

The larger the ratio of the bias current to the AC variations, the more linear the circuit is but the power efficiency (Ratio of AC power to DC power) becomes worse. As discussed in previous sections, **a linear amplifier based on BJTs requires that the collector current variations be limited to no more than 50% of the DC collector current ($v_{be}/V_{th}<0.5$)**. Therefore, amplifier's linearity is guarantied if and only if

$$I_{CQ} \geq 1.5 * i_{c\,max} = \frac{1.5 * v_{o\,max}}{\dfrac{R_C R_L}{R_C + R_L}} \tag{5.57}$$

Equations 5.53-5.57 can be plotted in the I_C-R_C plane as shown in the following figure. For this plot, the following parameters and design constraints were used: β=150, Z_i (eqn. 5.52) $\approx$150 kΩ, R_S=10 kΩ, R_L=10 kΩ, V_{omax}=1 V_{peak} and V_{CC}= 5V. In Figure 5.56, equation 5.55b is plotted for 3 different amplifier's gain (A_V=-5, -7.5 and -10). Notice that the acceptable solution region is quite limited compared with the one discussed in the previous example. In fact, the optimal solution is determined by the intersection of curves corresponding to equations 5.55b (that determines the amplifier's gain) and equation 5.57 (that guaranties linearity), but inside of the acceptable region. For instance, there is not any acceptable solution for voltage gain greater than –5. However, solutions can be found for smaller voltage gains.
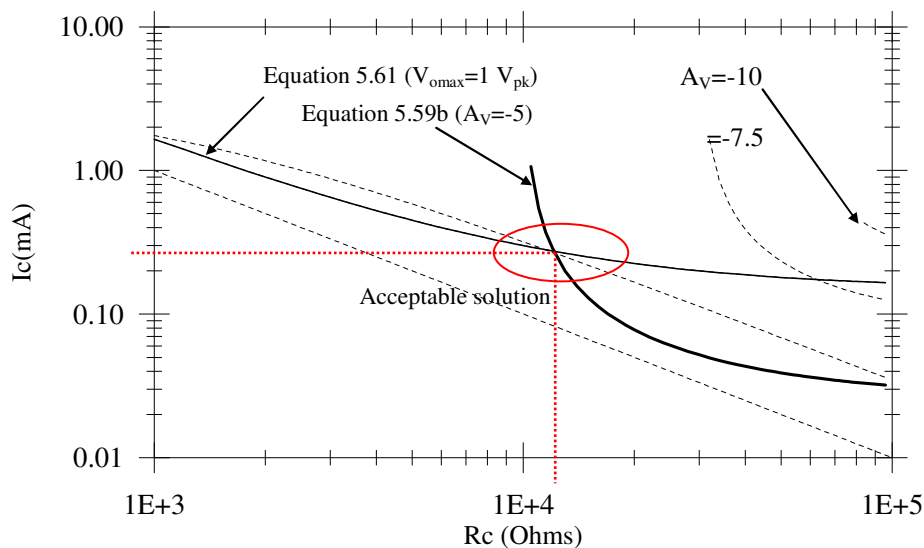
Fig. 5.56.

The main limitation of the circuit comes from the required input impedance ($z_i \approx \beta R_E$). This constraint requires to increase the resistance attached to the emitter R_E hence requiring even larger resistances at the collector terminal to afore the required voltage gain. This fact further limits the use of large collector current since large DC voltage drops across the emitter and collector resistances must be avoided, otherwise we do not have room for signal swing.

The circuit has been simulated in SPICE; from fig. 5.56 the selected collector current is 300 µA, and the collector resistance is 10 kΩ. The schematic and component values are shown below. The resistors R_{B1} and R_{B2} were selected to be very large in order not to degrade the input impedance; R_B=460 kΩ is used. The final design is shown in figure below. The DC volategs are also shown to verify our assumptions. Since the β of the device is greater than the value used in the hand calculations, the collector current is roughly 290 µA. Before you run the simulations, please double check the DC operating point of the circuit; verify the V_{CE} voltage and the collector current.

The circuit was simulated in Pspice, and the transient response for a sinewave nput signal of 200 mV$_{pk}$ is shown in the followingn plot. The AC signal at the base terminal of the transistor has a DC component of 0.96 V, while the DC component of the output signal is around 1.5 V. The amplitude of the AC signal at the base is around 190 m V$_{pk}$, shown that the input impedance is close to 100 kΩ, as expected. The output voltage is close 0.92 V$_{pk}$, leading to an overall voltage gain of -4.6. The small voltage gain is smaller than the expected -5 V due to the attenuation factor at the input stage of the amplifier, not taken into account in equation 5.55a. Since R_S=10 kΩ and the input impedance is around 100 kΩ, there is an attenuation factor in that interface of 10k/(100k+10k)=0.909, leading to a theoretical voltage gain of -4.54, that fits very well with Spice results. The frequency response can also be obtained from Spice by using the AC-analysis option; although the magnitude and phase repsonses are not shown, we encourage the reader to obtain that plot; it will be found that the amplifier's bandwidth (-3 dB frequency) is in the range of 100 MHz; for the design examples discussed in section 5.7, amplifier's bandwidth is around 20-30 MHz. This is another property of the circuits, the bandwidth is smaller for high-gain amplifiiers.

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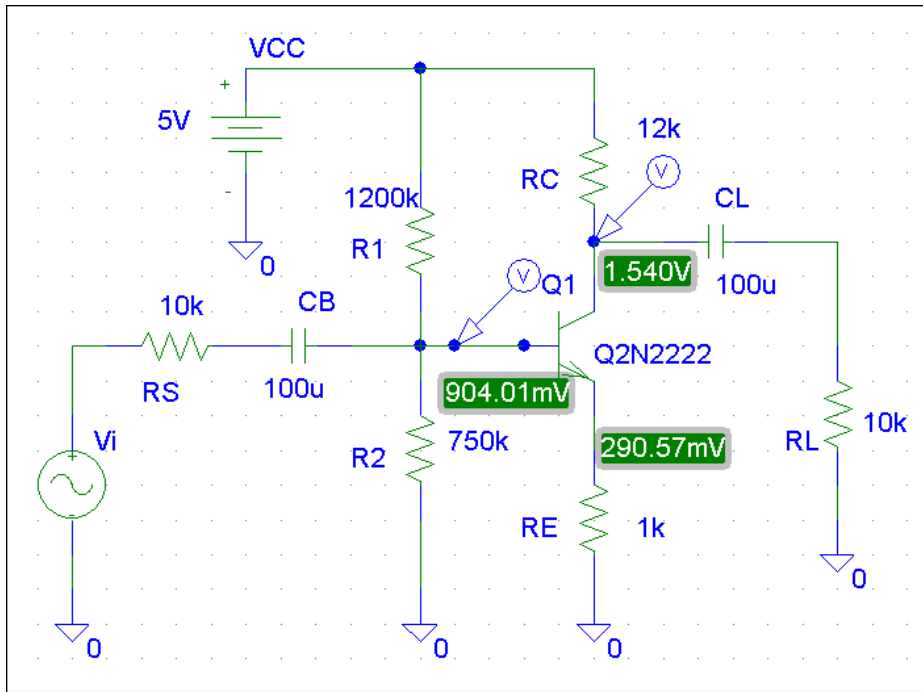
5.57. Common-emitter amplifier with emitter degeneration resistor RE to have more robust solution and better linearity performances.
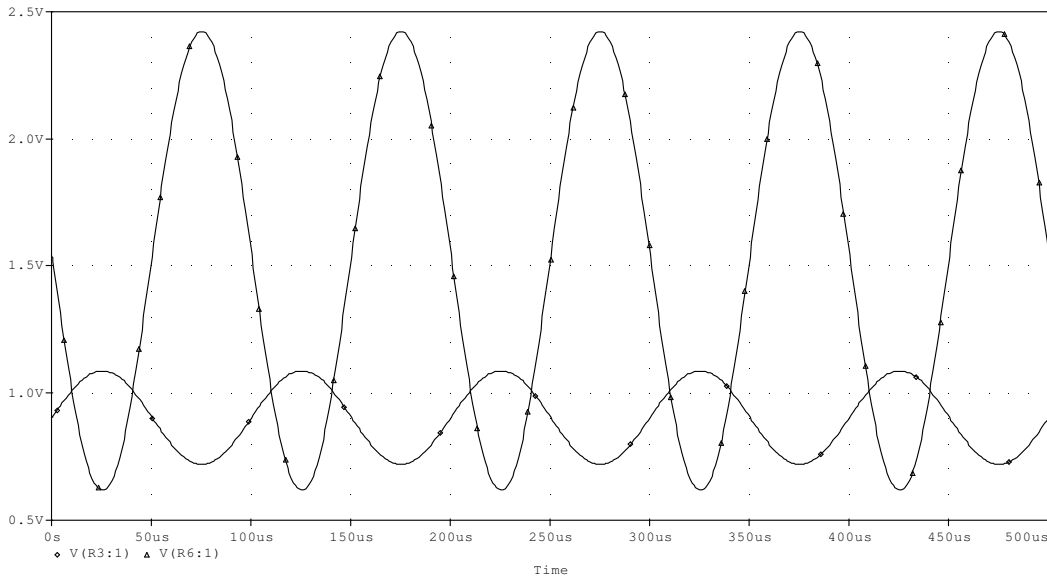
5.58. Spice results for an input signal of 200 mV$_{pk}$. Voltage gain is –4.6 V/V.

The amplifier's linearity can also be tested through the use of Spice transient simulation options. The first 3 harmonic distortions are depicted in the following plot. It can be seen that the fundamental component is close to 0.9 volts while the second harmonic component is around 10 mV, leading to a HD2 of around -40 dB. The third harmonic component is even smaller, roughly

2 mV; hence HD3 is around -54 dB. An interesting question here is why the circuit is very linear if the input voltage is around 200 mV?
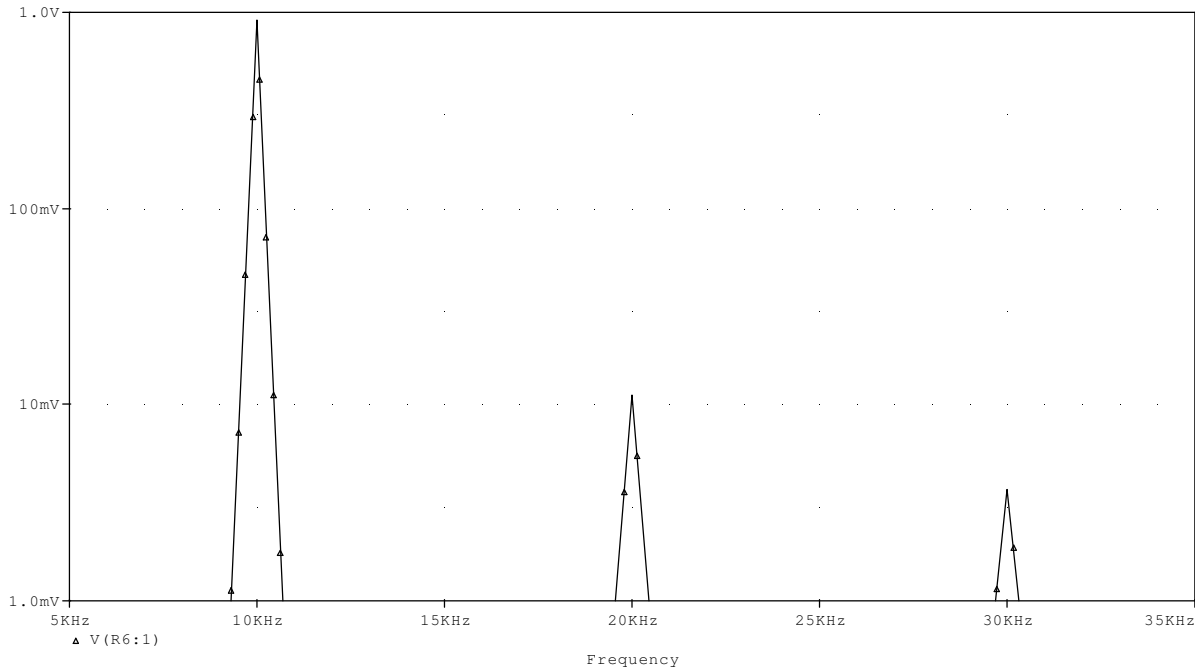
5.59. Spectral analysis of the collector waveform. The second harmonic component is nearly 10 mV (HD2~ -40 dB) and the third one is roughly 2 mV (HD3~ -54 dB).

Although the input voltage is very large, an important benefit of the emitter degeneration is that the voltage swing at the emitter terminal reduces drastically the base-emitter voltage. Let us consider the equivalent circuit, which is similar to the one shown in figure 5.19. The base-emitter voltage can be computed as

$$v_{be} = \frac{r_e}{r_e + R_E} v_b = \left(\frac{z_i}{z_i + R_S} \right) \left(\frac{r_e}{r_e + R_E} \right) v_i \tag{5.58}$$

For the components and bias conditions used, the emitter resistance r_e=86 Ω. Therefore, the base-emitter voltage v_{be} is further attenuated by the effect of R_E, leading to

$$v_{be} = (0.9) \left(\frac{86}{86 + 1000} \right) v_i = 0.072 v_i \tag{5.59}$$

For an input voltage v_i of 200 mV$_{pk}$, the effective base-emitter voltage is around 14.5 mV$_{pk}$. This simple analysis helps us to understand the fundamentals of linearization, but it is quite inaccurate for the prediction of the harmonic distortion components; fortunately the circuit is much linear than the simplified model predicts.

To compute HD2 and HD3 for the amplifier with emitter degeneration, the large signal model has to be used, since the small signal model, by definition, does not includes the non-linear I_C-

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V_{BE} characteristics of the transistor. In appendix 5A is shown that the second and third harmonic distortion components are given by the following expressions

$$HD2 = \frac{k_2}{2}i_{c-pk} = \left(\frac{1}{4}\right)\left|\frac{1}{\left(1+\dfrac{R_EI_{CQ}}{v_{th}}\right)}\right|\left(\frac{i_{c-pk}}{I_{CQ}}\right) \tag{5.60}$$

$$HD3 = \frac{k_3}{4}i_{c-pk}^2 = \left(\frac{1}{24}\right)\left|\frac{1-\dfrac{2R_EI_{CQ}}{v_{th}}}{\left(1+\dfrac{R_EI_{CQ}}{v_{th}}\right)^2}\right|\left(\frac{i_{c-pk}}{I_{CQ}}\right)^2 \tag{5.61}$$

If the numerical values used in the previous example are used, then: $I_{CQ}R_E$=290 mV, $I_{CQ}R_E/V_{th}$=11.6 and HD2 and HD3 yields,

$$HD2 \cong 0.021\left(\frac{i_{c-pk}}{I_{CQ}}\right) \qquad \sim -40dB \quad if \ \frac{i_{c-pk}}{I_{CQ}}=0.5$$

$$HD3 \cong 0.0058\left(\frac{i_{c-pk}}{I_{CQ}}\right)^2 \qquad \sim -56 \ dB \ \ if \ \frac{i_{c-pk}}{I_{CQ}}=0.5$$

Notice that these values fit very well with the results obtained from Spice.
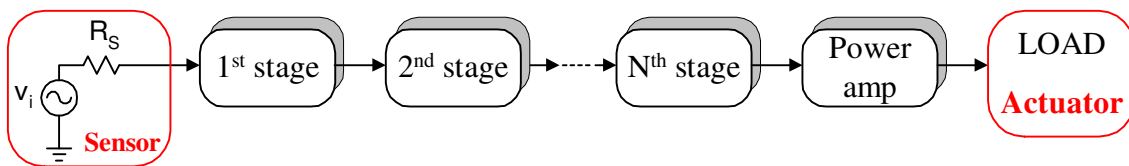
5.11. Multi-satge amplifiers.

Fig. 5.60

This section must include:

Amplifier's representation using input and output impedances, and transconductance or voltage gain
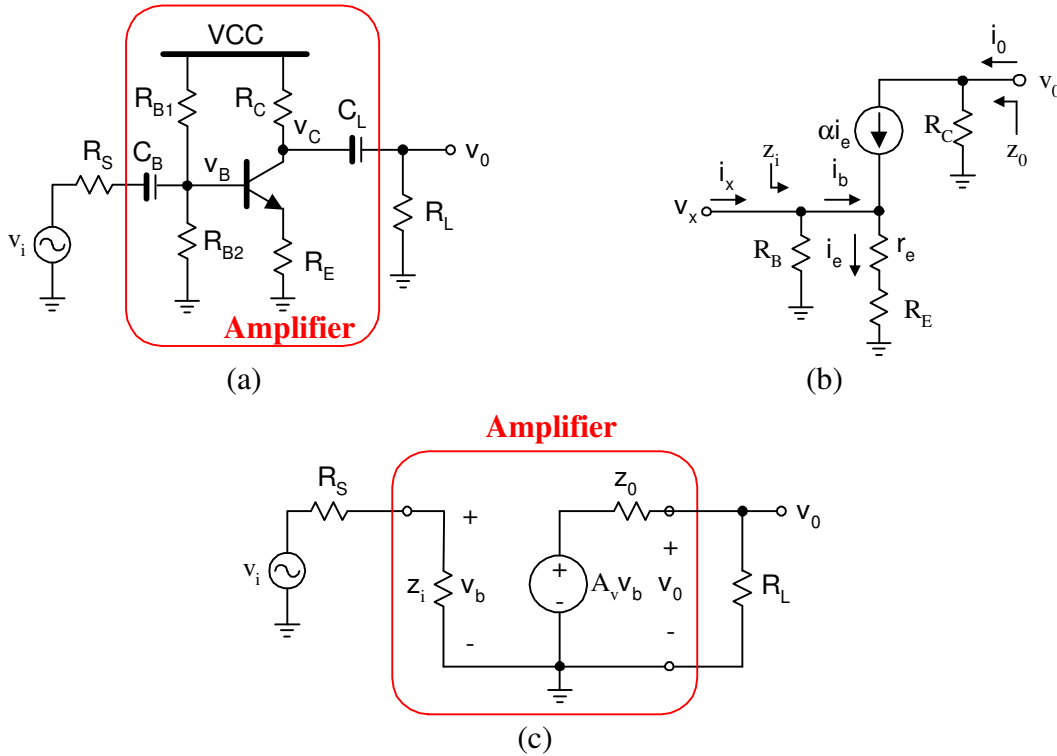
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(a)

(b)

(c)

Fig. 5.61.

Expressions for the input impedance, open-loop gain and output impedance will be given here.

In the following analysis we assume that $R_B >> \beta R_E >> r_\pi$. The input impedance of this topology is given as:

$$z_i = \left. \frac{v_b}{i_x} \right|_{R_L = \infty} = (r_e + R_E)(1 + \beta) \| R_B \cong (r_\pi + \beta R_E) \| R_B \tag{5.62}$$

Form the small signal analysis of the circuit, the amplifier's voltage gain is determined by the following expression

$$A_V = \left. \frac{v_0}{v_b} \right|_{R_L = \infty} = -\frac{g_m R_C}{1 + g_m R_E} = -\frac{\dfrac{I_{CQ}}{V_{th}} R_C}{1 + \dfrac{I_{CQ}}{V_{th}} R_E} \tag{5.63}$$

$$z_0 = \left. \frac{v_0}{i_0} \right|_{v_b = 0} = R_C \tag{5.64}$$
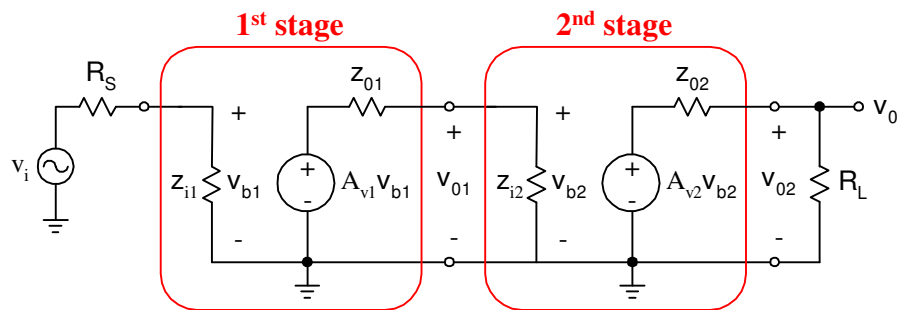
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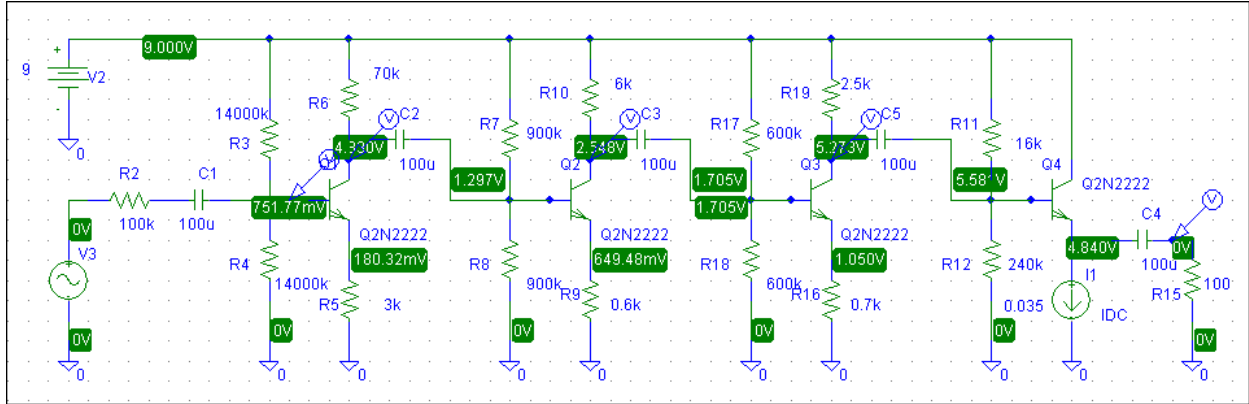
Two-stage amplifier: coupling effects

Fig. 5.62.

The overall transfer function is

$$A_{vT} = \left(\frac{z_{i1}}{R_S + z_{i1}} \right) \left(\frac{A_{v1}z_{i2}}{z_{o1} + z_{i2}} \right) \left(\frac{A_{v2}R_L}{z_{o2} + R_L} \right) \tag{5.64}$$
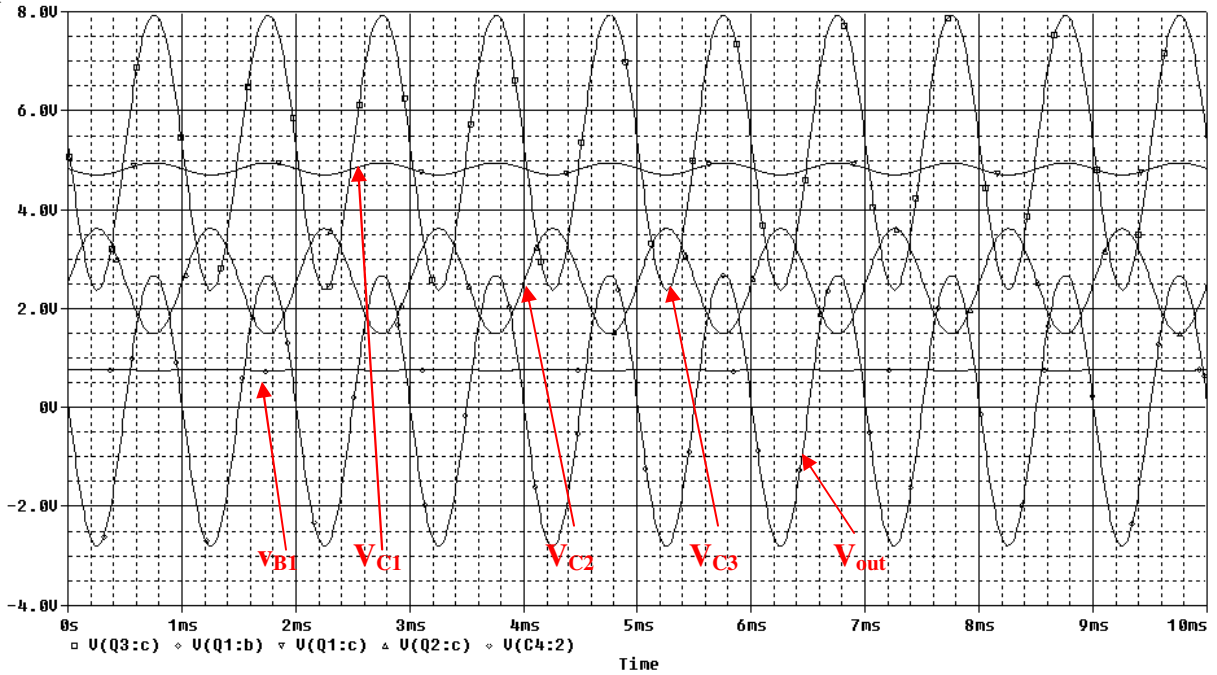
Then it is important to find out the input and output impedances of the standalone stages as well as the open-loop voltage gains.
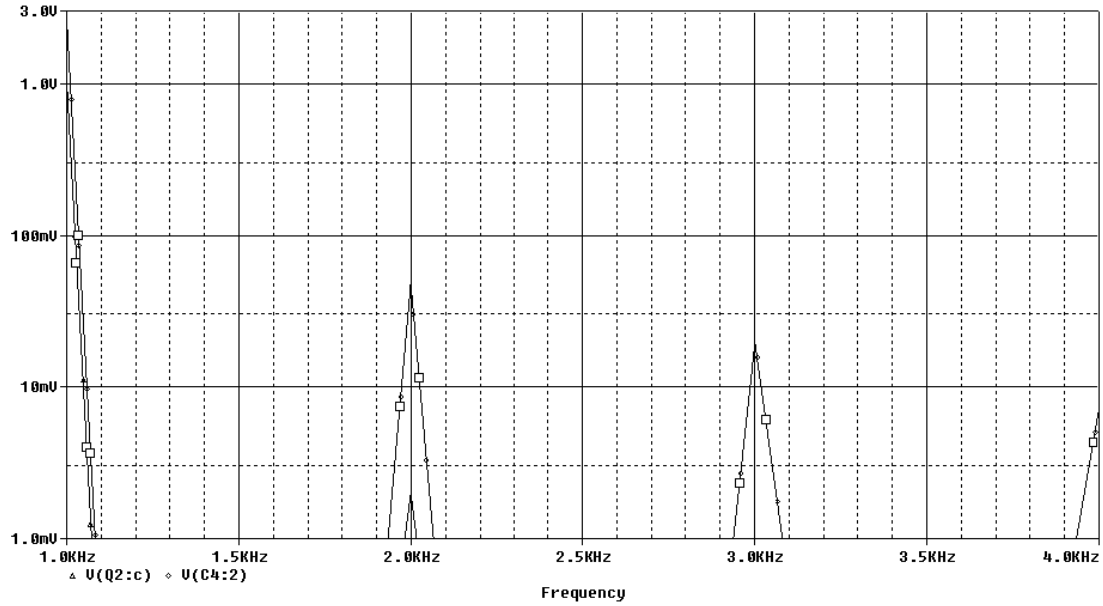
Design example of a multi-stage amplifier

Possible solution for assignment 6.

Spice results.

Spectrum of the waveforms at the collector of Q2 and amplifier's output. Overall output voltage is close to 2.8 V$_{pk}$; HD2≈30mV/2.8V=-39.4 dB, and HD3≈15mV/2.8V=-55.4 dB.

Appendix 5A:Harmonic distortion of a emitter degenerated common-emitter amplifier.

Let us consider again the circuit shown in figure 5.55. Although it is not completely true, let's assume that the voltage at the base v_B is a linear combination of the DC voltage VCC and the AC input signal vi, and it can be expressed as $v_B = V_B + v_b$.
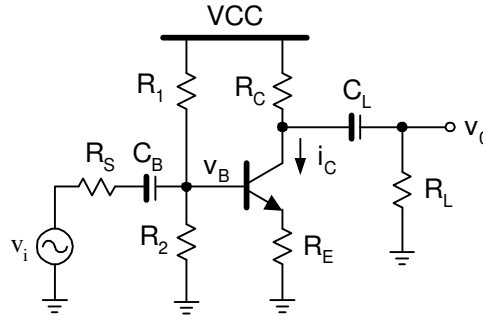
Fig. A5.1. Common-emitter amplifier with emitter degeneration resistor.

Notice that v_B is measured from the base terminal to ground. The collector current is generated by the base-emitter voltage ($v_{BE} = v_B - v_E = v_B - i_E R_E \approx v_B - i_C R_E$) and it is given by

$$i_C \cong I_S e^{\frac{v_B - i_C R_E}{v_{th}}} = I_S e^{\frac{V_B + v_b - (I_{CQ} + i_c)R_E}{v_{th}}} = \left(I_S e^{\frac{V_B - I_{CQ} R_E}{v_{th}}} \right)\left(e^{\frac{v_b - i_c R_E}{v_{th}}} \right) = \left(e^{\frac{v_b - i_c R_E}{v_{th}}} \right) I_{CQ} \qquad (A5.1)$$

Where it is assumed that β is high enough to consider α=1. This equation can also be expressed in the following form:

$$\frac{v_b - i_c R_E}{v_{th}} = \ln\left(\frac{i_C}{I_{CQ}} \right) = \ln\left(\frac{I_{CQ} + i_c}{I_{CQ}} \right) = \ln\left(1 + \frac{i_c}{I_{CQ}} \right) \qquad (A5.2)$$

where i_C is expressed as an addition of the DC component I_{CQ} and the non-linear AC component i_c. The function ln(x) stands for the natural logarithm of x. For small x, the function ln(1+x) can be expanded in a taylor series as $\ln(1+x) = x - 0.51x^2 + 0.34x^3 - \ldots$ Using this series into equation A5.2, leads to:

$$\frac{v_b - i_c R_E}{v_{th}} = \frac{i_c}{I_{CQ}} - 0.51\left(\frac{i_c}{I_{CQ}} \right)^2 + 0.34\left(\frac{i_c}{I_{CQ}} \right)^3 - .. \cong \frac{i_c}{I_{CQ}} - \frac{1}{2}\left(\frac{i_c}{I_{CQ}} \right)^2 + \frac{1}{3}\left(\frac{i_c}{I_{CQ}} \right)^3 - .. \qquad (A5.3)$$

To solve this equation is cumbersome and very often numerical results are employed. For the case $i_c < I_{CQ}$, the high-order terms can be ignored, and equation leads to

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$$\frac{v_b}{v_{th}} \cong \left(1+\frac{R_E I_{CQ}}{v_{th}}\right)\left(\frac{i_c}{I_{CQ}}\right)-\frac{1}{2}\left(\frac{i_c}{I_{CQ}}\right)^2+\frac{1}{3}\left(\frac{i_c}{I_{CQ}}\right)^3 \tag{A5.4}$$

This is a non-linear equation, and it is difficult to solve it; obviously numerical methods or Spice can give us the solutions. However, it is interesting to find first order solutions that help us to properly use the degrees of freedom we may have when a circuit is designed.

A practical, but not very precise, approach is introduced here. If the collector current i_c is considered to have 3 main harmonic distortion components, then it can always be expressed as

$$i_c = i_{c0}+k_2 i_{c0}^2+k_3 i_{c0}^3 \tag{A5.5}$$

where i_{c0} is the fundamental component of the collector current, and i_{c0}^2 and i_{c0}^3 are the result of second and third order non-linearities present in the amplifier. If we assume that the input signal v_b consists of an ideal tone as shown in the following plot. The output current i_c consists of several harmonics as depicted in the same figure, similar spectrums are obtained for i_{c0}^2 and i_{c0}^3.
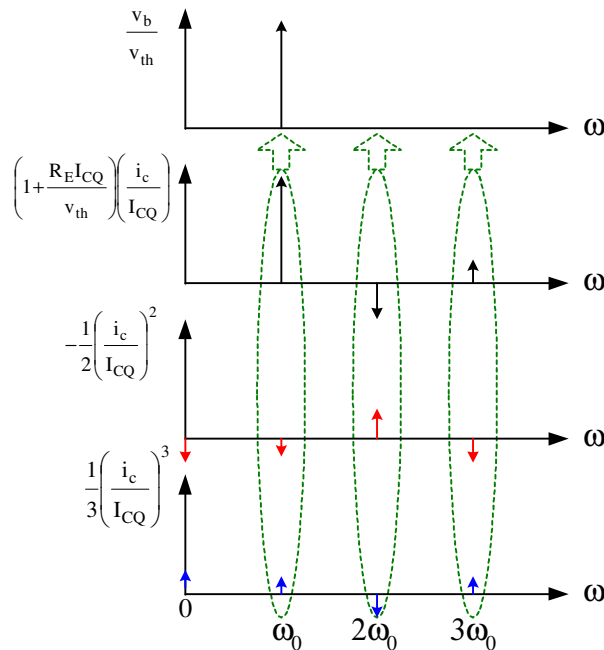

Fig. A5.2. Graphical interpretation of equation A5.6. The AC Input signal v_b consists of a single tone. i_c, i_c^2 and i_c^3 consists of fundamental tones at $\omega=\omega_o$ plus several harmonic components.

Then using expression A5.4 into equation A5.5 yields,

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$$\frac{v_b}{v_{th}} = \left\{ \begin{array}{l} \left(1+\dfrac{R_E I_{CQ}}{v_{th}}\right)\left(\dfrac{i_{c0}+k_2 i_{c0}{}^2+k_3 i_{c0}{}^3}{I_{CQ}}\right) - \dfrac{1}{2}\left(\dfrac{i_{c0}+k_2 i_{c0}{}^2+k_3 i_{c0}{}^3}{I_{CQ}}\right)^2 + \\[6mm] + \dfrac{1}{3}\left(\dfrac{i_{c0}+k_2 i_{c0}{}^2+k_3 i_{c0}{}^3}{I_{CQ}}\right)^3 - .. \end{array} \right. \qquad (A5.6a)$$

or

$$\frac{v_b}{v_{th}} = \left\{ \begin{array}{l} \left(1+\dfrac{R_E I_{CQ}}{v_{th}}\right)\left(\dfrac{i_{c0}}{I_{CQ}}\right) - \\[6mm] + \left(\left(1+\dfrac{R_E I_{CQ}}{v_{th}}\right)(k_2 I_{CQ})-\dfrac{1}{2}+..\right)\left(\dfrac{i_{c0}}{I_{CQ}}\right)^2 + \\[6mm] + \left(\left(1+\dfrac{R_E I_{CQ}}{v_{th}}\right)(k_3 I_{CQ}{}^2)-(k_2 I_{CQ})+\dfrac{1}{3}-..\right)\left(\dfrac{i_{c0}}{I_{CQ}}\right)^3 \end{array} \right. \qquad (A5.6b)$$

Although it is very difficult to find the exact solution for this equation, simple observations lead to very simple and relatively accurate results. First at all, the spectrum of the right hand side term is proportional to v_b, and in a first approximation it consists of a single tone if an ideal sinusoidal is applied to the amplifier. Hence, the combination of all spectrums at the right-hand side of equation A5.6 must consists of a single tone as well, because the two spectrums have to be equal. According to equation A5.6, the right hand side coefficients of this expression must be zero with the exception of the first one, which defines the small signal transconductance of the amplifier. Therefore, it follows that

$$\frac{v_b}{v_{th}} = \left(1+\frac{R_E I_{CQ}}{v_{th}}\right)\left(\frac{i_{c0}}{I_{CQ}}\right)$$

$$\left(1+\frac{R_E I_{CQ}}{v_{th}}\right)(k_2 I_{CQ})-\frac{1}{2}\cong 0 \qquad (A5.7)$$

$$\left(1+\frac{R_E I_{CQ}}{v_{th}}\right)(k_3 I_{CQ}{}^2)-(k_2 I_{CQ})+\frac{1}{3}\cong 0$$

Thus, the small signal transconductance becomes

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$$i_{c0} = \left(\frac{\left(\frac{I_{CQ}}{v_{th}} \right)}{1 + \frac{R_E I_{CQ}}{v_{th}}} \right) v_b = \left(\frac{g_m}{1 + g_m R_E} \right) v_b \tag{A5.8}$$

Which fits with the small signal analysis done for this circuit in previous sections; overall voltage gain is obtained by taking into account the input voltage divider $(z_i/(z_i+R_S))$, the small signal transconductance gain given by A5.6, and the overall load resistance. The overall linearized voltage gain is then obtained as

$$v_0 = -\left(\frac{z_i}{z_i + R_S} \right) \left(\frac{g_m R_C \| R_L}{1 + g_m R_E} \right) v_i \tag{A5.9}$$

This expression is similar to the one given in table 5.1. The coefficients k_2 and k_3 are computed as

$$k_2 = \left(\frac{1}{2} \right) \left(\frac{1}{\left(1 + \frac{R_E I_{CQ}}{v_{th}} \right) (I_{CQ})} \right) \tag{A5.10}$$

$$k_3 = \left(\frac{-1 + 3k_2 I_{CQ}}{3} \right) \left(\frac{1}{\left(1 + \frac{R_E I_{CQ}}{v_{th}} \right) (I_{CQ}{}^2)} \right) = \left(\frac{1}{6} \right) \left(\frac{1 - \frac{2R_E I_{CQ}}{v_{th}}}{\left(1 + \frac{R_E I_{CQ}}{v_{th}} \right)^2 (I_{CQ}{}^2)} \right)$$

Therefore, the second and third harmonic distortions can be approximated as follows

$$HD2 = \frac{k_2}{2} i_{c-pk} = \left(\frac{1}{4} \right) \left(\frac{1}{\left(1 + \frac{R_E I_{CQ}}{v_{th}} \right)} \right) \left(\frac{i_{c-pk}}{I_{CQ}} \right) \tag{A5.11}$$

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$$HD3 = \frac{k_3}{4} i_{c-pk}^2 = \left(\frac{1}{24}\right)\left(\frac{1 - \frac{2R_E I_{CQ}}{v_{th}}}{\left(1 + \frac{R_E I_{CQ}}{v_{th}}\right)^2}\right)\left(\frac{i_{c-pk}}{I_{CQ}}\right)^2 \qquad\qquad (A5.12)$$

If the numerical values used in the previous example are used, then: $I_{CQ}R_E$=290 mV, $I_{CQ}R_E/V_{th}$=11.6 and HD2 and HD3 yields,

$$HD2 \cong 0.021\left(\frac{i_{c-pk}}{I_{CQ}}\right) \qquad \sim -40\text{dB if } \frac{i_{c-pk}}{I_{CQ}} = 0.5$$

$$HD3 \cong 0.0058\left(\frac{i_{c-pk}}{I_{CQ}}\right)^2 \qquad \sim -56 \text{ dB if } \frac{i_{c-pk}}{I_{CQ}} = 0.5$$

These values are in good agreement with the ones obtained from Spice.

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